Dr.G.R.Damodaran College of Science

(Autonomous, affiliated to the Bharathiar University, recognized by the UGC)Re-accredited at the 'A' Grade Level by the **NAAC** and ISO 9001:2008 Certified
CRISL rated 'A' (TN) for MBA and MIB Programmes

II BCA [2016 - 2019]
Semester III
Allied : Microprocessor and Assembly Language Programming - 306D
Multiple Choice Questions.

1. The Microarchitecture of a processor is its _____ architecture.
   A. Circuit
   B. Processor
   C. internal
   D. parallel
   ANSWER: C

2. In ALP,Binary instructions are abbreviated as _____.
   A. assembly language.
   B. machine language.
   C. binary patterns.
   D. mnemonics.
   ANSWER: D

3. Prefetched instruction are held in the _____
   A. LIFO
   B. FIFO
   C. FILO
   D. LILO
   ANSWER: B

4. How many building blocks are present in a microcomputer system?
   A. 4
   B. 6
   C. 8
   D. 10
   ANSWER: A

5. Which bus is unidirectional?
   A. data bus.
   B. control bus.
   C. system bus.
   D. address bus.
   ANSWER: D

6. Multiplex is a combination of _____.
   A. data & control bus
   B. control& address bus
   C. address& data bus
   D. data& control bus
   ANSWER: C

7. Which among the following are the pointer registers?
   A. base pointer & stack pointer.
   B. index pointer & decision pointer.
   C. service pointer & stack pointer.
   D. stack pointer & index pointer.
   ANSWER: A

8. How many internal register are there in 8086 micro processor?
   A. 14
   B. 13
   C. 18
   D. 16
   ANSWER: B

9. Maximum capacity of four memory segments provide _____bytes of active memory.
   A. 255
   B. 256k
   C. 512k
   D. 164k
   ANSWER: B

10. _____is an example for volatile memory.
   A. RAM.
   B. ROM.
   C. CD.
   D. DVD.
   ANSWER: A

11. Instruction pointer is similar to _____.
   A. program counter.
   B. micro controller.
   C. status counter.
   D. instruction code.
   ANSWER: A

12. The stack pointer is refered as _____
   A. STP
   B. SP
   C. STK
   D. None of the above

ANSWER: B

13. AL operations are used for _____.
A. arithmetic & linear
B. arithmetic&logic.
C. arithmetic &long
D. none of the above
ANSWER: B

14. BX stands for_____.
A. translate.
B. byte addition
C. byte multiply.
D. byte divide.
ANSWER: A

15. RISC stands for _____.
A. Reduced Instruction System Computer
B. Reduction Instruction Set Car
C. Recycled Instruction Set Computer
D. Refined Instruction Set Computer
ANSWER: A

16. Collection of instruction are called_____.
A. mnemonics.
B. instruction tags.
C. instruction sets.
D. opcodes.
ANSWER: C

17. Format for instruction set is_____.
A. mnemonics opcode operand.
B. data opcode operand.
C. opcode data operand.
D. opcode operand mnemonics.
ANSWER: A

18. Which mnemonis copy bytes to destination?
A. MOV.
B. POP.
C. LEA.
D. LES.
ANSWER: A

19. Which of the following operation is used to copy specified mode to top of the stack_____.
A. POP.
B. LES.
C. PUSH.

D. .LDS.
ANSWER: C

20. A_____ copy word from stack to all register.
A. POP.
B. OUT.
C. IN.
D. XCHG.
ANSWER: A

21. A operation used to exchange byte or exchange word is_____.
A. IN
B. XGHG
C. PUSH
D. LEA
ANSWER: B

22. An _____load DS register and other specified register from memory.
A. LDS.
B. LES.
C. DSL.
D. LEA.
ANSWER: A

23. RISC stands for_____.
A. Reduced Integrated Set Computer.
B. Resource Instruction Set Computer.
C. Resource Instruction System Computer.
D. Reduced Instruction Set Computer.
ANSWER: D

24. A _____operation is used to compare two specified byte.
A. CEP
B. CMP
C. AAS
D. CBB
ANSWER: B

25. A_____ shift bit left 0 in LSB.
A. SHL
B. SHR
C. SLH
D. SSL
ANSWER: A

26. An_____and operands to update flags but dont change operands.
A. TEST.
B. AND.

C. NAND.
D. NOR.
ANSWER: A

27. An_____ASCII adjust after multiplication.
A. AAA.
B. AMA.
C. AMI.
D. AAM.
ANSWER: D

28. _____is used to a procedure or subprogram save return address on stack.
A. CALL.
B. CLC.
C. CLD.
D. CLI.
ANSWER: A

29. An _____ jump if flag CF=1.
A. JNSE.
B. JNSC.
C. JNS.
D. JNC.
ANSWER: B

30. Microprocessors can be classified according to _____,
A. The type of application
B. The application
C. The type
D. none
ANSWER: A

31. An_____ jump if not signed.
A. JNSE.
B. JNSC.
C. JNS.
D. JNC.
ANSWER: C

32. The _____ used to set carry flag=1.
A. STE
B. STC
C. STP
D. SCT
ANSWER: B

33. A_____ is used to do anything until interrupt is reset.
A. HLT.

B. HALT.
C. HLTE.
D. HALTE.
ANSWER: A

34. A _____ is used for not a program.
A. NOT.
B. NO.
C. ESC.
D. NOP.
ANSWER: D

35. The _____ used for clear interrupt enable control flag to 0. .
A. ENB.
B. CLT.
C. CIE.
D. IEF.
ANSWER: B

36. Out of 16-bit register within the 8088 _____ flags are used.
A. 12
B. 13
C. 10
D. 9
ANSWER: D

37. The_____ indicates conditions that are provided as results of executes as logical instructions.
A. sign flag.
B. overflow flag.
C. status flag.
D. zero flag.
ANSWER: C

38. Three important flag bits together are called _____.
A. union flag.
B. controlled flag.
C. parity flag.
D. carry flag.
ANSWER: B

39. An _____ is set if there is any carry out from lower nibble to higher nibble.
A. auxiliary carry
B. carry flag
C. carry auxiliary flag
D. parity flag
ANSWER: A

40. A_____is reset, any request at INTR is ignored.

A. trap flag.
B. overflow flag.
C. interrupt flag.
D. sign flag.
ANSWER: C

41. When _____ is set it indicates that signed result is out of range.
A. trap flag.
B. overflow flag.
C. interrupt flag.
D. sign flag.
ANSWER: B

42. How many addressing modes are available?
A. 7
B. 8
C. 6
D. 10
ANSWER: A

43. Combining base address mode and index address mode we can get _____.
A. indexing base address mode.
B. base index addressing mode.
C. based indexing address mode.
D. based index addressing mode.
ANSWER: B

44. The MSB of the result is copied into _____.
A. sign flag.
B. carry flag.
C. zero flag.
D. parity flag.
ANSWER: A

45. The _____ is set if result of arithmetic or logic operation is zero.
A. sign flag.
B. zero flag
C. parity flag.
D. carry flag.
ANSWER: B

46. BIU stands for?
A. Bus Interface Units.
B. Block interfacing unit.
C. Bus Interrupt unit
D. Block interrupt unit.
ANSWER: A

47. The_____ moves from source to destination & destination to source.
A. control bus.
B. data bus.
C. system bus.
D. address bus.
ANSWER: B

48. Multiprocessor communicate and operates in_____.
A. binary numbers.
B. real numbers.
C. whole numbers.
D. float numbers.
ANSWER: A

49. A _____ used for compliment state of carry flag.
A. CMC.
B. CLC.
C. CLD.
D. CCF
ANSWER: A

50. The _____ set interrupt unable flag=1.
A. SII.
B. SIU.
C. STD.
D. STI.
ANSWER: D

51. The 8086 based micro processor system can have maximum of _____ memory locations.
A. 240.
B. 230.
C. 220.
D. 210.
ANSWER: C

52. The category of reprogrammable microprocessors represents_____.
A. The class of applications
B. The class
C. The applications
D. The class of applications 1
ANSWER: A

53. The unsigned word integer data type in 8088 can support decimal numbers in the range_____.
A. 0 to 356.
B. 0 to 256.
C. 0 to 65,535.
D. 0 to 55,535.
ANSWER: C

54. The unsigned byte integer data type in 8088 can support decimal numbers in the range_____.
A. 0 to 128.
B. 0 to 255.
C. 0 to 65,535.
D. 0 to 35,565.
ANSWER: B

55. In protected mode _____address lines are active.
A. 18.
B. 30.
C. 20.
D. 22.
ANSWER: B

56. Protected mode addresses are _____bits long.
A. 20
B. 32
C. 18
D. 64
ANSWER: B

57. The 8088 microprocessor directly process the data expressed in a _____.
A. Number of different data types
B. Number of different data
C. Number of different types
D. Number types
ANSWER: A

58. The _____produces the control signals for the I/O subsystem.
A. 8288 bus controller
B. 8298 bus controller
C. 8828 bus controller
D. 8988 bus controller
ANSWER: A

59. The interrupt request recognized by 8088 signals the fact to_____.
A. external circuitry.
B. I/O interface.
C. internal circuitry.
D. memory device.
ANSWER: A

60. External circuitry should put an _____type number on bus lines AD0 through AD7.
A. 8 bit.
B. 16 bit.
C. 32 bit.
D. 64 bit.

ANSWER: A

61. The distance of the data path between the MPU and interrupt interface is _____ bits in length.
A. 16 bit.
B. 18 bit.
C. 32 bit.
D. 64 bit.
ANSWER: A

62. A _____is applied as an input to a bus arbiter.
A. LOCK.
B. INTA.
C. SSO.
D. DEN.
ANSWER: A

63. The 8086 microprocessor are capable of implementing any combination upto 256 interrupts they are divided into_____.
A. 2 groups.
B. 4 groups.
C. 5 groups.
D. 6 groups.
ANSWER: C

64. A_____identifies the lowest priority interrupt.
A. type 0.
B. type 225.
C. type 5.
D. type 100.
ANSWER: B

65. A_____identifies the starting location of service routines in program memory.
A. addressing pointer.
B. stack pointer .
C. Instruction pointer.
D. overflow pointer.
ANSWER: A

66. Which pointer is used to identify the starting location of the non-askable interrupt service routine ?
A. 2 pointer .
B. 1 pointer.
C. 3 pointer.
D. 5 pointer.
ANSWER: A

67. The 8088 can process data as either_____.
A. unsigned or signed integer
B. unsigned integer

C. signed integer
D. integer only
ANSWER: A

68. Each of the 256 pointers in the vctor table require _____of memory.
A. 2 bytes.
B. 2.4 bytes.
C. 6 bytes.
D. 8 bytes.
ANSWER: B

69. The 27 pointers 5 to 31 are used to _____.
A. identify starting location.
B. represent reserved portions.
C. user availability .
D. find the interrupts.
ANSWER: B

70. A _____identifies the program memory segment in which the service routines reside.
A. base address .
B. 8288 bus controller.
C. data bus.
D. address bus.
ANSWER: A

71. STI Stands for_____.
A. set interrupt enable flag
B. interrupt enable flag
C. enable flag
D. interrupt flag
ANSWER: A

72. CLI Stands for _____.
A. clear interrupt enable flag
B. interrupt enable flag
C. clear enable flag
D. interrupt flag
ANSWER: A

73. The last signal line involved in the host processor interface is the_____.
A. A0.
B. AD1
C. AD0.
D. A1.
ANSWER: A

74. The overflow error is an error condition_____.
A. similar to divide error

B. to divide error
C. error
D. similar error
ANSWER: A

75. The _____carries the physical address generated by the CPU and selects the memory location to be accessed.
A. address bus.
B. data bus.
C. control bus.
D. memory address.
ANSWER: A

76. The _____transfers data between the CPU registers and the selected memory location.
A. address bus.
B. data bus
C. control bus
D. memory address
ANSWER: B

77. Reset RD=DEN='logic1'is used to_____.
A. END the read-bus-cycle.
B. to initiate reading data into CPU.
C. to select memory interface.
D. to let data pass.
ANSWER: A

78. The data from the memory is read by sampling the data bus at the end of _____.
A. T1.
B. T2.
C. T3.
D. T4.
ANSWER: C

79. The _____is introduced for the support of multiprocessor environment in Maximum mode.
A. bus controller.
B. address bus.
C. data bus.
D. control bus.
ANSWER: A

80. The_____ signal is used to control the access of even or odd memory banks of 8086 system.
A. bank high enable.
B. data enable.
C. acknowledge signal.
D. ready.
ANSWER: A

81. Maximum mode status codes needs to be active to generate control signals from_____.
A. bus controller.
B. address bus.
C. data bus.
D. control bus.
ANSWER: A

82. Which of the following interrupts have the lowest priority?
A. Hardware interrupt.
B. Nonmaskable interrupt.
C. Software interrupt.
D. Internal interrupts and exceptions.
ANSWER: A

83. Microprocessor is fabricated on single chip using _____.
A. MOS.
B. ALU.
C. CPU
D. None.
ANSWER: A

84. The table is located by the system, at a memory location described by the_____.
A. Interrupt Descriptor Table Address Register.
B. data register.
C. segment register.
D. pointer register.
ANSWER: A

85. A_____causes external interrupts to be enable
A. interrupt enable flag.
B. carry flag.
C. parity flag.
D. zero flag.
ANSWER: A

86. The _____instruction should be used after each arithmetic instruction where there is a possibility of an overflow.
A. INTO.
B. INT
C. HLT.
D. WAIT.
ANSWER: A

87. The divide error flow function represents_____.
A. execution of division instructions
B. division instructions
C. execution of instructions
D. instructions

ANSWER: A

88. When the PIC is configured through software for the cascade mode, the _____ line is used as an input.
A. SP/EN.
B. SP.
C. EN.
D. INT
ANSWER: A

89. Which are the eight interrupt inputs of the PIC are labeled?
A. IR0 through IR7.
B. IR1 through IR8.
C. D0 through D7.
D. D1 through D8.
ANSWER: A

90. The breakpoint function can also be used to_____.
A. implement a software diagnostic tool
B. a software diagnostic tool
C. implement a software
D. diagnostic tool
ANSWER: A

91. Bug means_____.
A. a logical error in a program.
B. semantic error
C. a difficult syntax error in a program.
D. duplicate of a program.
ANSWER: A

92. The part of machine level instruction, which tells the central processor what was to be done is_____.
A. operation code.
B. MOV
C. INX
D. INS
ANSWER: A

93. The 82C37A carries _____ pins.
A. 48.
B. 28.
C. 40.
D. 20.
ANSWER: C

94. DMA channels has_____ address register.
A. 12

B. 8
C. 4
D. 2
ANSWER: D

95. 82C55A carries _____ pins.
A. 40
B. 28
C. 20
D. 48
ANSWER: A

96. Current address register is a _____ bit register.
A. 16
B. 32
C. 8
D. 4
ANSWER: A

97. Mass register is a _____bit register.
A. 8.
B. 4
C. 16
D. 32
ANSWER: B

98. How many modes of operation in 8254A ?
A. 5
B. 6
C. 4
D. 2
ANSWER: B

99. The 82C37A operates through _____.
A. software.
B. hardware.
C. hardware and software.
D. peripheral devices.
ANSWER: A

100. The Status register is a _____ bit register.
A. 4.
B. 6
C. 8
D. 16
ANSWER: C

101. The number of bytes data to be transfer during DMA operation the value is _____.

A. base word count register.
B. current word count register.
C. base address register.
D. current address register.
ANSWER: A

102. Temporary word count register is a _____ bit register.
A. 6.
B. 4
C. 8
D. 16
ANSWER: D

103. The 82C54 is a _____bit integrated circuit.
A. 24
B. 20
C. 48
D. 64
ANSWER: A

104. Command register is a _____.
A. 4 bit register.
B. 6 bit register.
C. 8 bit register.
D. 16 bit register.
ANSWER: C

105. Data transfer between the microprocessor and peripherals takes place through _____.
A. input ports.
B. output ports.
C. input and output ports.
D. address ports.
ANSWER: A

106. Temporary register is a_____.
A. 4 bit register.
B. 6 bit register.
C. 16 bit register.
D. 8 bit register.
ANSWER: D

107. The 82C55A has _____I\O lines
A. 24.
B. 16.
C. 48.
D. 32.
ANSWER: A

108. The mode register is a _____.
A. 16 bit register .
B. 6 bit register.
C. 8 bit register.
D. 4 bit register.
ANSWER: B

109. The Base word count register is a _____.
A. 6 bit register.
B. 8 bit register.
C. 16 bit register.
D. 4 bit register.
ANSWER: C

110. There are _____ 16 bit counters in 82C54
A. 3
B. 4
C. 5
D. 2
ANSWER: A

111. In 82C54,the data bus buffer shows _____.
A. tri state 8 bit direction.
B. tri state 16 bit direction.
C. tri state 32 bit direction.
D. tri state 64 bit direction.
ANSWER: A

112. Request register is a _____.
A. 6 bit register.
B. 4 bit register.
C. 8 bit register.
D. 16 bit register.
ANSWER: B

113. The 82C55A operates with _____ power supply
A. +5.
B. +10.
C. +3.
D. +7.
ANSWER: A

114. Current word count register is a _____ bit register.
A. 4.
B. 6.
C. 8.
D. 16.
ANSWER: D

115. There are _____ 16 bit counters in 82C54.
A. 3.
B. 4.
C. 6.
D. 2.
ANSWER: A

116. The 82C54 has _____ address input pins.
A. 1.
B. 3.
C. 2.
D. 6.
ANSWER: C

117. The Base address register is a _____ bit register.
A. 4.
B. 16.
C. 8.
D. 6.
ANSWER: B

118. In 82C55A the chip select input is connected to _____ in the system.
A. I/O ports.
B. control register.
C. address decoder .
D. data bus.
ANSWER: C

119. BCD Stands for_____.
A. binary coded decimal
B. binary decimal
C. coded decimal binary
D. binary coded
ANSWER: A

120. The serial communication interface permits _____ to be transferred between two units using data lines.
A. control signals.
B. data
C. address.
D. input/output.
ANSWER: B

121. The spectrum of embedded control application requires_____.
A. a variety of system features
B. asystem features
C. a system features

D. a variety of features
ANSWER: A

122. The 8088 has_____.
A. 4 general purpose registers
B. 3 general purpose registers
C. 2 general purpose registers
D. 1 general purpose registers
ANSWER: A

123. BP Stands for_____.
A. base pointer
B. basic pointer
C. base only
D. pointer
ANSWER: A

124. Serial communication interface is also called as _____.
A. serial communication port
B. serial communication device
C. communication data
D. communication port
ANSWER: A

125. The serial communication interface is used to connect ____ to a micro computer.
A. address unit.
B. peripheral unit.
C. data unit.
D. control unit.
ANSWER: B

126. The DACK acknowledge lines are the____ from the controller.
A. output.
B. request.
C. input.
D. acknowledge.
ANSWER: A

127. The 82C54 provides _____ signals to other device.
A. timing.
B. bus.
C. control.
D. address.
ANSWER: A

128. ASCII Stands for_____
A. american code for information interchange
B. standard code for information interchange

C. american standard code for information interchange
D. american information interchange
ANSWER: C

129. The internal register in 82C37A are divided into _____ groups.
A. 4.
B. 3.
C. 2.
D. 5.
ANSWER: C

130. The bidirectional data lines are used to transfer count ,control and ____ word between microprocessor and 82C54.
A. comman
B. status.
C. temporary.
D. mass.
ANSWER: B

131. Command register programs the operation of the _____.
A. address.
B. data.
C. peripheral device.
D. control.
ANSWER: D

132. Sychronization bit at the end of the character is called as _____.
A. stop bit.
B. start bit.
C. parity bit.
D. space bit.
ANSWER: A

133. Mode register has _____ basic mode of operation.
A. 5.
B. 3.
C. 2.
D. 4.
ANSWER: D

134. The single mask register allows individual DMA channels to be _____.
A. masked off.
B. masked on.
C. mask.
D. off.
ANSWER: A

135. When more than one 82C37A is present in the system _____ mode is use

A. cascade.
B. demand transfer.
C. block transfer.
D. single transfer.
ANSWER: A

136. The data lines are _____.
A. bidirectional.
B. unidirectional
C. multiplexer.
D. demultiplexer.
ANSWER: A

137. The 82C37A activates the memory read and memory write _____ using DMA operations.
A. command output signals.
B. command input signals.
C. control output signals.
D. control input signals.
ANSWER: C

138. The ADSTB output signals is used to ____ high order address by and data in 82C37A.
A. control.
B. demultiplex.
C. multiplex.
D. request.
ANSWER: B

139. In 82C37A,the READY input signal is used to extend _____.
A. address cycle.
B. input cycle.
C. output cycle.
D. bus cycle.
ANSWER: D

140. The _____ mode automatically transfer the no of bytes indicated by the count register.
A. cascade
B. demand transfer
C. block transfer
D. single transfer
ANSWER: C

141. Temporary address register is a _____ bit register.
A. 4.
B. 6.
C. 8.
D. 16.
ANSWER: D

142. Pentium I is a successor of _____.
A. 80486.
B. 80386.
C. 80786.
D. 80286.
ANSWER: A

143. The _____have a large versatile instruction set that supports many complex addressing modes.
A. 8086.
B. 8087.
C. 8085.
D. 8085&8086.
ANSWER: A

144. The MPU of the 80486 family are best described as_____.
A. CRIS
B. RIS
C. IMUL.
D. IMUL.
ANSWER: A

145. Pentium I is implemented in the year_____.
A. 1993.
B. 1992.
C. 1990.
D. 1994.
ANSWER: A

146. The internal cache memory unit of the 80486DX is _____in size and caches both code and data.
A. 2bytes.
B. 4bytes.
C. 8bytes.
D. 10bytes.
ANSWER: C

147. How many transistors does Pentium I have?
A. 3.4 to 3.6 million transistors.
B. 3.1 to 3.3 million transistors.
C. 3.8 to 4.2 million transistors.
D. 4.6 to 4.8 million transistors.
ANSWER: B

148. The speed of Pentium III is _____.
A. 450MHZ to 1.4 GHZ.
B. 250MHZ to 1.0GHZ.
C. 150MHZ to 1.3GHZ.
D. 150MHZ to 1.5GHZ.
ANSWER: A

149. The _____works on clock speed 800MHZ.
A. Pentium I.
B. Pentium III.
C. Pentium IV.
D. Pentium I and Pentium II.
ANSWER: D

150. The _____microprocessor supports both a math co processor and cache memory.
A. 8279.
B. 80486.
C. 8255
D. 80386.
ANSWER: D

151. 80486 MP is tightly pipelined by how many transistors_____.
A. 2 million transistors.
B. 3 million transistors.
C. 4million transistors.
D. 8 million transistors.
ANSWER: A

152. A _____ processor is typically characterized as having small instruction set limited addressing modes and single clock execution for instructions.
A. IDI
B. IMUL
C. RIS
D. CRIS
ANSWER: C

153. During system operation the _____memory contains recently used data or both.
A. RAM.
B. ROM.
C. cache memory.
D. EPROM.
ANSWER: C

154. Pentium I has _____8kb cache units.
A. four.
B. two.
C. eight.
D. three.
ANSWER: B

155. The intervals of no bus activity which occur between bus cycle are known as_____ .
A. Temporary state.
B. Permanent state.
C. Idle states.

D. Active state.
ANSWER: C

156. In the _____ the p6 microarchitecture is enriched with an addition 70 instructions.
A. pentium I.
B. pentium III.
C. pentium IV.
D. pentium II.
ANSWER: B

157. How many bytes of instructions code does instruction stream queue permit?
A. 32bytes.
B. 16 bytes.
C. 128 bytes.
D. 64 bytes.
ANSWER: B

158. In _____processor,it provide two separate buses (ie.) cache bus and system memory bus
A. pentium II.
B. pentium I.
C. pentium IV.
D. pentium III.
ANSWER: A

159. The bus unit is responsible for performing all _____ operations.
A. external bus. .
B. internal bus.
C. internal control bus.
D. effective address bus
ANSWER: A

160. A _____has both 32bit internal registers and a 32bit external data bus.
A. 80386DX.
B. 80386SX.
C. 80486DX.
D. 80486SX.
ANSWER: A

161. The 80386 family of micro processors represent the first _____bit members of Intel popular micro processor architecture.
A. 32 bit.
B. 64 bit.
C. 128 bit.
D. 16 bit.
ANSWER: A

162. RIAM Stands for_____.
A. Register Indirect Addressing Mode

B. Indirect Addressing Mode
C. Register Addressing Mode
D. Addressing Mode
ANSWER: A

163. How many functional units does 80386 have?
A. 8 functional units.
B. 6 functional units.
C. 16 functional units.
D. 4 functional units.
ANSWER: B

164. BAM Stands for_____.
A. Bsaed Addressing Mode
B. Addressing Mode
C. Bsaed Addressing
D. Bsaed Addressing Mode1
ANSWER: A

165. The _____ is the 80386DX interface.
A. interface unit.
B. bus unit .
C. execution unit.
D. internal bus .
ANSWER: B

166. The MPU and cache chips are separately _____.
A. packaged ICS.
B. ICS.
C. M
D. external bus.
ANSWER: D

167. The _____microprocessor are implemented with multiple, simultaneously operating processing units.
A. 80486SX.
B. 80386SX.
C. 80486DX.
D. 80386DX.
ANSWER: A

168. The errors that can be pointed out by the compiler_____.
A. syntax errors.
B. semantic errors.
C. logical errors.
D. I/O error.
ANSWER: A

169. C is_____.
A. an assembly language.
B. a third generation high level language.
C. a machine language.
D. a gaming program.
ANSWER: B

170. A graph prepared by a computer_____.
A. printing.
B. is the piece of information to use.
C. is a soft copy.
D. plotting.
ANSWER: B

171. Which of the following does not represent on I/O device?
A. speaker which beeps.
B. joystick.
C. plotter.
D. ALU.
ANSWER: D

172. The communication line between the CPU, memory and peripherals is called a_____.
A. bus.
B. line.
C. medi
D. coaxial cable.
ANSWER: A

173. Memories which can be read only are called_____ memories.
A. RAM.
B. ROM
C. PROM.
D. EPROM.
ANSWER: B

174. One thousand bytes represent a_____.
A. megabyte.
B. gigabyte.
C. kilobyte.
D. tetra Byte.
ANSWER: C

175. The language that the computer can understand and execute is called_____.
A. machine language.
B. application software.
C. system program.
D. human Language
ANSWER: A

176. A step by step procedure used to solve a problem is called_____.
A. operating system.
B. algorithm.
C. application Program.
D. program.
ANSWER: B

177. Terminal is a_____.
A. device to give power supply to computer.
B. point at which data enters or leaves the computer.
C. the last instruction in a program.
D. any input /output device.
ANSWER: B

178. Multiple choice examination answer sheets can be evaluated automatically by_____.
A. optical Mark Reader.
B. optical Character Reader. .
C. magnetic tape reader
D. magnetic ink character reader.
ANSWER: A

179. A computer cannot BOOT if it does not have the_____.
A. compiler.
B. loader.
C. operating system.
D. assembler.
ANSWER: C

180. WAN hardware includes_____.
A. multiplexors and routers.
B. EDF.
C. bridge and modems.
D. antenn
ANSWER: A

181. Third generation computers_____.
A. were the first to use built-in error detecting device.
B. used transistors instead of vacuum tubes.
C. were the first to use neural network.
D. used IC.
ANSWER: D

182. A Winchester disk is a_____.
A. disk stack.
B. removable disk.
C. flexible disk.
D. CD ROM.

ANSWER: A

183. A computer can be defined as an electronic device that can be (choose the most precise Definition) .
A. carry out arithmetical operation.
B. carry out logical function.
C. accept and process data using a set of stored instructions.
D. present information on a VDU.
ANSWER: C

184. The Central Processing Unit_____.
A. is operated from the control panel.
B. is controlled by the input data entering the system.
C. controls the auxiliary storage unit.
D. controls all input, output and processing.
ANSWER: D

185. Computer follows a simple principle called GIGO which means_____.
A. garbage input good output.
B. garbage in garbage out.
C. great instructions great output.
D. good input good output.
ANSWER: B

186. The term baud is a measure of the_____.
A. speed at which data travels over the communication line.
B. memory capacity.
C. instruction execution time.
D. size.
ANSWER: A

187. A bootstrap is_____.
A. a memory device.
B. a device to support the computer.
C. a small initialization program to start up a computer.
D. an error correction technique.
ANSWER: C

188. Which of the following is not hardware?
A. magnetic tape.
B. printer.
C. VDU terminal.
D. assembler.
ANSWER: D

189. Pick out the wrong definition.
A. access time time needed to access the output.
B. EDP acronym for Electronic Data Processing.
C. COBOL a language used for business data processing.

D. control unit heart of a computer.
ANSWER: A

190. SMTP Stands for_____.
A. switched mode power supply.
B. simple mode power supply.
C. simple mail transfer protocol.
D. small message transfer protocol.
ANSWER: B

191. A smart card is also called a_____.
A. integrated circuit.
B. integrated chip.
C. implemented cards.
D. implemented chips.
ANSWER: A

192. Smart cards contain a _____ security system.
A. safe.
B. interfering.
C. tamper-resistant.
D. tampere
ANSWER: C

193. There are _____ broad categories of smart cards.
A. four.
B. three.
C. five.
D. two.
ANSWER: D

194. An _____ Chips do not need an external programming voltage.
A. PROM.
B. EEPROM.
C. EPROM.
D. ROM.
ANSWER: B

195. MOS PROCESSOR 2 microprocessor is used in which industry?
A. mechanical.
B. computers.
C. mobiles.
D. aeronautical.
ANSWER: D

196. Early pc used which chip to interface keyboard?
A. intel.
B. intel 8042.

C. intel 8056.
D. intel pentium.
ANSWER: B

197. Name the device which interfaces keyboard and computers?
A. keyboard interface.
B. keyboard controller.
C. keyboard circuit.
D. keyboard chip.
ANSWER: B

198. In computers with PS/2 connector keyboard is interfaced with _____.
A. printer.
B. CPU.
C. mouse.
D. monitor.
ANSWER: C

199. Keyboards receive _____from microcontroller.
A. rays.
B. magnetic lines.
C. signals.
D. scan codes.
ANSWER: D

200. Direct addressing mode is similar to_____.
A. Immediate addressing
B. Immediate addressing1
C. Immediate addressing2
D. Immediate addressing3
ANSWER: A

201. CS Stands for _____.
A. code segment
B. code segment1
C. code segment2
D. code segment3
ANSWER: A

202. Normally, _____matrix keyboard is used.
A. 4*4.
B. 7*7.
C. 2*2.
D. 8*8.
ANSWER: D

203. When a key is pressed only _____ in the port goes high.
A. byte.

B. bit.
C. 2 byte.
D. 2 bit.
ANSWER: B

204. In which pc keyboards single microprocessor takes care of hardware and software?
A. IBM.
B. windows.
C. xp.
D. linux.
ANSWER: A

205. In refrigerators, micro processors are used for_____.
A. controlling temperature.
B. voltage control.
C. automatic on/off.
D. current control.
ANSWER: A

206. Seven segment display uses _____.
A. LED and LC
B. LED ONLY.
C. LCD ONLY.
D. electronic waves.
ANSWER: A

207. To check the row of the pressed key in the keyboard, one of the row is made _____
A. high.
B. low.
C. active.
D. set.
ANSWER: A

208. MIPS Stands for _____.
A. instructions per second
B. million instructions
C. million of instructions per second
D. million instructions per second
ANSWER: D

209. The Direct access method used for magnetic tape is_____
A. direct.
B. random.
C. sequential.
D. indirect.
ANSWER: C

210. The language that the computer can understand and execute is called_____.

A. machine language.
B. application software.
C. system program.
D. High level Language.
ANSWER: A

211. The difference between memory and storage is that the memory is_____ and Storage is_____.
A. temporary, permanent .
B. permanent, temporary.
C. slow, fast.
D. volatile, non-volatile.
ANSWER: A

212. Which of the Following holds the ROM, CPU, RAM and expansion cards?
A. hard disk.
B. floppy disk .
C. mother board
D. PC Slot.
ANSWER: C

213. The language that the computer can understand and execute is called _____.
A. machine language.
B. application software.
C. system program.
D. high level language.
ANSWER: A

214. Which of the following devices can be used to directly input printed text?
A. OCR.
B. OMR.
C. MICR.
D. scanner.
ANSWER: A

215. A floppy disk contains_____.
A. circular tracks only.
B. sectors only.
C. both circular tracks and sectors.
D. no sectors.
ANSWER: C

216. CD-ROM is a_____.
A. semiconductor memory.
B. memory registers.
C. magnetic memory.
D. chip register.
ANSWER: D

217. Actual execution of instructions in a computer takes place in_____.
A. ALU.
B. control Unit.
C. storage unit.
D. MPU.
ANSWER: A

218. Which of the following is used as a primary storage device?
A. magnetic tape.
B. PROM.
C. floppy disk.
D. MM
ANSWER: B

219. Information retrieval is faster from_____.
A. floppy disk.
B. magnetic tape.
C. hard disk.
D. US.
ANSWER: C

220. Execution of two or more programs by a single CPU is known as_____.
A. multiprocessing.
B. time sharing.
C. multiprogramming.
D. copying.
ANSWER: C

221. Pentium I is a successor of _____.
A. 80486.
B. 80386.
C. 80786.
D. 80286.
ANSWER: A

222. The _____have a large versatile instruction set that supports many complex addressing modes.
A. 8086.
B. 8087.
C. 8085.
D. 8088
ANSWER: A

223. The MPU of the 80486 family are best described as_____.
A. CRIS
B. RIS
C. IMUL.
D. IDIV.

ANSWER: A

224. Pentium I is implemented in the year_____.
A. 1993.
B. 1992.
C. 1990.
D. 1994.
ANSWER: A

225. The internal cache memory unit of the 80486DX is _____in size and caches both code and data.
A. 2bytes.
B. 4bytes.
C. 8bytes.
D. 10bytes.
ANSWER: C

226. How many transistors does Pentium I have?
A. 3.4 to 3.6 million transistors.
B. 3.1 to 3.3 million transistors.
C. 3.8 to 4.2 million transistors.
D. 4.6 to 4.8 million transistors.
ANSWER: B

227. DI Stands for _____.
A. Destination Index
B. Destination
C. Index
D. Destination Index II
ANSWER: A

228. The _____works on clock speed 800MHZ.
A. Pentium I&III.
B. Pentium III&IV.
C. Pentium IV&I.
D. Pentium I and Pentium II.
ANSWER: D

229. The _____microprocessor supports both a math co processor and cache memory.
A. 8279.
B. 80486.
C. 8255
D. 80386.
ANSWER: D

230. 80486 MP is tightly pipeline by how many transistors_____.
A. 2 million transistors.
B. 3million transistors.
C. 4million transistors.

D. 8 million transistors.
ANSWER: A

231. A _____ processor is typically characterized as having small instruction set limited addressing modes and single clock execution for instructions.
A. IDI.
B. IMUL.
C. RIS.
D. CRIS.
ANSWER: C

232. During system operation the _____memory contains recently used data or both.
A. RAM.
B. ROM.
C. cache memory.
D. EPROM.
ANSWER: C

233. Pentium I has _____8kb cache units.
A. four.
B. two.
C. eight.
D. three.
ANSWER: B

234. The intervals of no bus activity which occur between bus cycle are known as_____ .
A. Temporary state.
B. Permanent state.
C. Idle states.
D. Active state.
ANSWER: C

235. In the _____ the p6 microarchitecture is enriched with an addition 70 instructions.
A. pentium I.
B. pentium III.
C. pentium IV.
D. pentium II.
ANSWER: B

236. How many bytes of instructions code does instruction stream queue permit?
A. 32bytes.
B. 16 bytes.
C. 128 bytes.
D. 64 bytes.
ANSWER: B

237. In 8086,a word is a combination of _____bits.
A. 8.

B. 4.
C. 16.
D. 32.
ANSWER: C

238. The bus unit is responsible for performing all _____ operations.
A. external bus.
B. internal bus.
C. internal control bus.
D. effective address bus.
ANSWER: A

239. A _____has both 32bit internal registers and a 32bit external data bus.
A. 80386DX.
B. 80386SX.
C. 80486DX.
D. 80486SX.
ANSWER: A

240. The 80386 family of micro processors represent the first _____bit members of Intel's popular micro processor architecture.
A. 32 bit.
B. 64 bit.
C. 128 bit.
D. 16 bit.
ANSWER: A

241. Which device with its 32bit internal register and 16 bit data bus provide a lower performance MPU for the 80386 based microcomputer system?
A. 80486SX.
B. 80486DX.
C. 80386DX.
D. 80386SX.
ANSWER: C

242. How many functional units do 80386 have?
A. 8
B. 6
C. 16
D. 4
ANSWER: B

243. The virtual _____ was not supported by the protected mode of the 80286 microprocessor.
A. 8086mode.
B. 8085mode.
C. 8088mode.
D. 8087mode.
ANSWER: A

244. The _____ is the 80386DX's interface.
A. interface unit.
B. bus unit.
C. execution unit.
D. internal bus.
ANSWER: B

245. The MPU and cache chips are separately _____.
A. packaged ICS.
B. ICS.
C. Sequential bus.
D. external bus.
ANSWER: D

246. The _____microprocessor are implemented with multiple, simultaneously operating processing units.
A. 80486SX.
B. 80386SX.
C. 80486DX.
D. 80386DX.
ANSWER: A

247. Which of the following does not represent on I/O device?
A. speaker which beeps.
B. joystick.
C. plotter.
D. ALU.
ANSWER: D

248. The communication line between the CPU, memory and peripherals is called a_____.
A. bus.
B. line.
C. medium.
D. coaxial cable.
ANSWER: A

249. Memories which can be read only are called_____ memories.
A. RAM.
B. ROM.
C. PROM.
D. EPROM.
ANSWER: B

250. The index registers are used to _____.
A. Hold offset addresses
B. Hold addresses
C. offset addresses

D. Hold offset addresses1
ANSWER: A

Staff Name
kavitha.v.r.